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Study and Analysis of NewMultilevel Inverter Topology

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Abstract: *Multilevel inverter technology has emerged recently as a very important alternative in the area of high-power medium-voltage energy control. This paper presents modeling and simulation of a single phase simplified eleven-level inverter (SELl). Multilevel inverter offers high power capability. Its performance is highly superior to that of conventional two-level inverter due to reduced harmonic distortion, lower electromagnetic interference and higher dc link voltage. Recent advances in technology have realized the cascaded inverters with separate DC sources to have a considerable reduction in switching losses and the ability to control the harmonic content.The elementary concept of a multilevel converter to achieve higher power to use a series of power semiconductor switches with several lower voltage dc source to perform the power conversion by synthesizing a staircase voltage waveform.Simulations of eleven level of the proposed inverter topology along with MATALAB simulation results are presented.*

Keywords: *Simplified Eleven-level Inverter (SELl), Flying Capacitor, Active neutral point clamped.*

I. Introduction

The earliest concept of multilevel topology consisted of a series connection of multiple DC sources with switchis connected to different level of the voltage source[1], and a simple 3-level realization is showed in Fig.1 (a) [2]. Animprovement that can equalize the stress on the switches resulted in the structure shown in Fig.1 (b) which is called stacked commutation cell or 3-pole cell. This topology uses series connection of switches which show more complexity of the commutation and control for higher level converters. At the same time, neutral-point-clamped (NPC) structure was developed[2, 3]. A 3-level NPC topology shown in Fig.1 (c) can be considered as the particular way of implementing 3-pole cell topology[4]: two inner switches and two clamping diodes are used to play the role of middle level track. This structure can be easily extended to higher level called diode clamped multilevel converter [5] known as the most popular multilevel topology. Nevertheless, some drawbacks exist for this topology, such as rapidly increasing number of clamping diodes for higher level, neutral point voltage balancing problem, indirect clamping of the inner devices, unequal distribution of losses in semiconductor devices, etc. To overcome these disadvantages, flying capacitorswere introduced as the clamping devices[6], then hybrid converter clamped with diode and capacitor was presented, shown in Fig.1 (d).

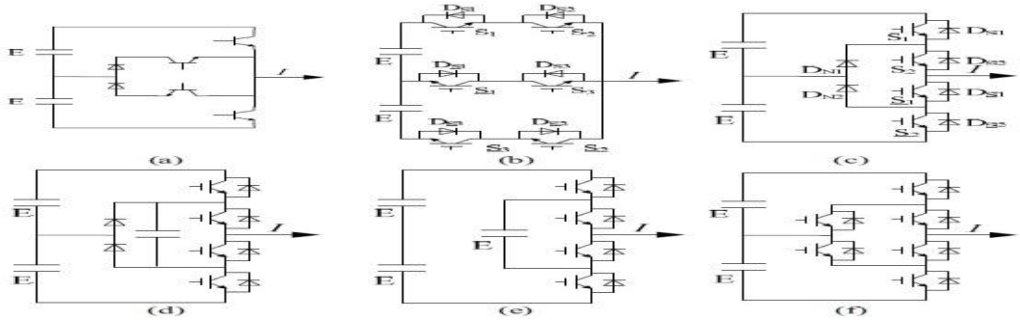

Fig. 1. Basic topologies

Then flying-capacitor converter (also called multicell) which uses only the flying capacitors as clamping devices was presented in [7] and discussed comprehensively by Meynard[4, 8, 9], shown in Fig.1 (e). As the capacitors can provide extra capability during power output, the voltage synthesis in a flying-capacitor converter presents more flexibility than a diode-clamped converter. Furthermore, the more redundancy of switch combination is beneficial for balancing voltages of the flying capacitors. Nevertheless, its control is more

complicated, and an excessive number of storage capacitors are required for higher level. Considering that the size of flying capacitor is inversely proportional to the switching frequency, the NPC structure is more advantageous than flying-capacitor structure in the field of low and moderate frequencies. Another topology called active neutral-pointclamped (ANPC) was also proposed to avoid the problems of indirect clamping and unequal loss distribution of power devices in NPC converters [10, 11]. As is shown in Fig.1 (f), additional active switches antiparallel to the NPC diodes are used to ensure the equal voltage sharing of the series-connected NPC diodes. With appropriate control, losses distribution can be more balanced, that can give substantial increase of the output power or switching frequency.

II. Multilevel Inverter Topologies

The term 'Multilevel' has been coined to emphasize the ability to increase the instantaneous voltage levels in steps, accomplished by addition of components in series.Multilevel inverter is based on the fact that sine wave can be approximated to a stepped waveformsynthesized output waveform has more steps, producing a very fine stair case wave and approaching very closely to the desired sine wave. It can be easily understood that as motor steps are included in the waveform the harmonic distortion of the output wave decrease, approaching zero as the number of levels approaches infinity. Hence Multi-level inverters offer a better choice at the high power end because the high volt- ampere ratings are possible with these inverters without theproblems of high dv/dt and the other associated ones.

Generally, the output waveform of the multilevel inverter is generated from different voltage sources obtained from the capacitor voltage sources. In the past two decades, several multilevel voltage source converters have been introduced. In that some of the topologies are popular and some are not popular.

The basic three types of multilevel topologies used are
(A) Cascaded inverter with separate DC sources.
(B)Flying capacitors multilevel inverter or capacitorclamped multilevel inverter.
(C) Diode clamped multilevel inverters.

A.Cascaded Inverters with Separate DC Source
The concept of this inverteris based on connecting H-bridge inverters in series to get a sinusoidal voltage output.The output voltage is the sum of thevoltagethatisgeneratedby eachcell.The number ofoutputvoltage levelsare2*n*+1,where *n* is the number of cells. The switching angles can be chosen in such away thatthetotalharmonicdistortionisminimized. One oftheadvantagesofthistypeofmultilevelinverteristhatitneedslessnumberof componentscomparativetotheDiodeclamped ortheflying capacitor,sothepriceandthe weight of theinverterislessthanthatofthetwoformertypes.Fig.2showscascaded H-bridge multilevel inverter.Theswitchingangles calculation method that is used in this inverteris thesameasfor the previous multilevel inverters.An*n*levelcascadedH-bridgemultilevelinverterneeds2(*n*-1)switchingdeviceswhere*n*is the number ofthe outputvoltagelevel.

i) Advantages of cascaded multi-level inverter
1.Require the least number of components among all multi-level converter to achieve the same number voltage levels.
2.Modulized circuit layout and packaging it possible becauseeach level has the structure, and there are no extra clamping diodes or voltage balancing capacitors
3.Soft switching can be used in this structure to avoid bulky and lossyresistor, capacitor, diode, snubbers.

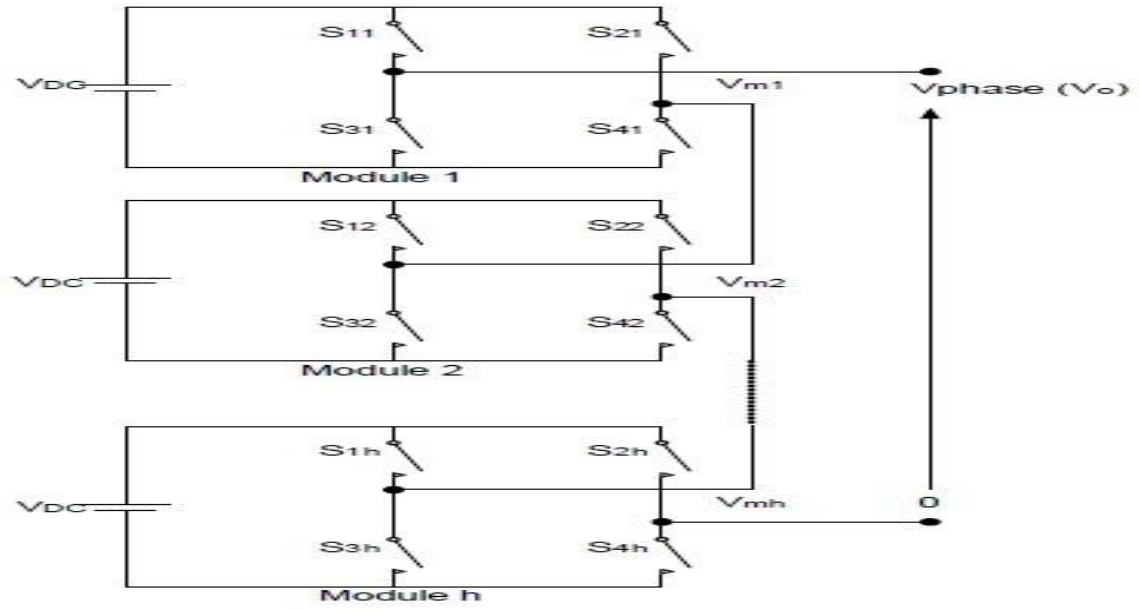

Fig. 2One phase of a cascaded H-bridge multilevel inverter

ii) Disadvantages of cascaded multi-level inverter
1.Limited to certain applications where separate DC sources are available.

B. Flying Capacitor (FC) Multilevel Inverter
Thisinverterusescapacitorstolimitthevoltageofthepowerdevices.Theconfigurationof theflying capacitormultilevelinverterislikeadiodeclampedmultilevelinverterexceptthat capacitorsare used todividetheinputDCvoltage.The voltage overeachcapacitor and each switch isV_{dc}.Fig.3 shows the flyingcapacitor three level inverter. Multilevel FC converter topology was developed in the 1990s and it uses several floating capacitors instead of clamping diodes, to share the voltage stress among devices, and to achieve different voltage levels in the output voltage. Depending on the voltage of the floating capacitors, the number of voltage levels change.

C. Diode Clamped Multilevel Inverters
Themainconceptofthisinverteristousediodestolimitthepowerdevicesvoltagestress.
ThevoltageovereachcapacitorandeachswitchisV_{dc}.An*n*levelinverterneeds(*n*-1) voltage sources, 2(*n*-1) switchingdevices and(*n*-1)(*n*-2)diodes. The maximum output voltage in the output is half of the DC source.
It is a drawback of the diode clamped multilevel inverter. This problem can be solved by using a two times voltage source or cascading two diode clamped multilevel inverters. Fig. 4 show the diode clamped three level inverter. This topology with a high number of levels has a high unequal distribution of the losses among semiconductors which forces a derating of the power devices, and also a reduction of the lifetime of the power semiconductors. The comparison of each topology is show in the Table I.

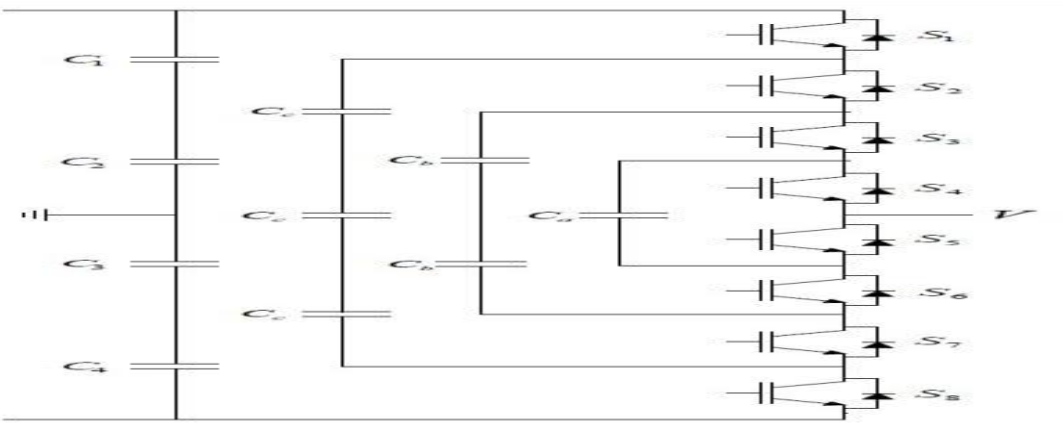

Fig. 3One phase of a 5-level Flying capacitor multilevel inverter

Table I DEVICES REQUIRED IN DIFFERENT TOPOLOGIES

Topologies (5-level)	Switches (main and clamping)	Diodes(antiparallel and clamping)	Clamping capacitors
Generalized	20	20	6
Diode-Clamped	8	20	0
Flying Capacitor	8	8	6
Capacitor-Clamped	8	20	6
Novel Topology (Used in Current Paper)	4	8	2

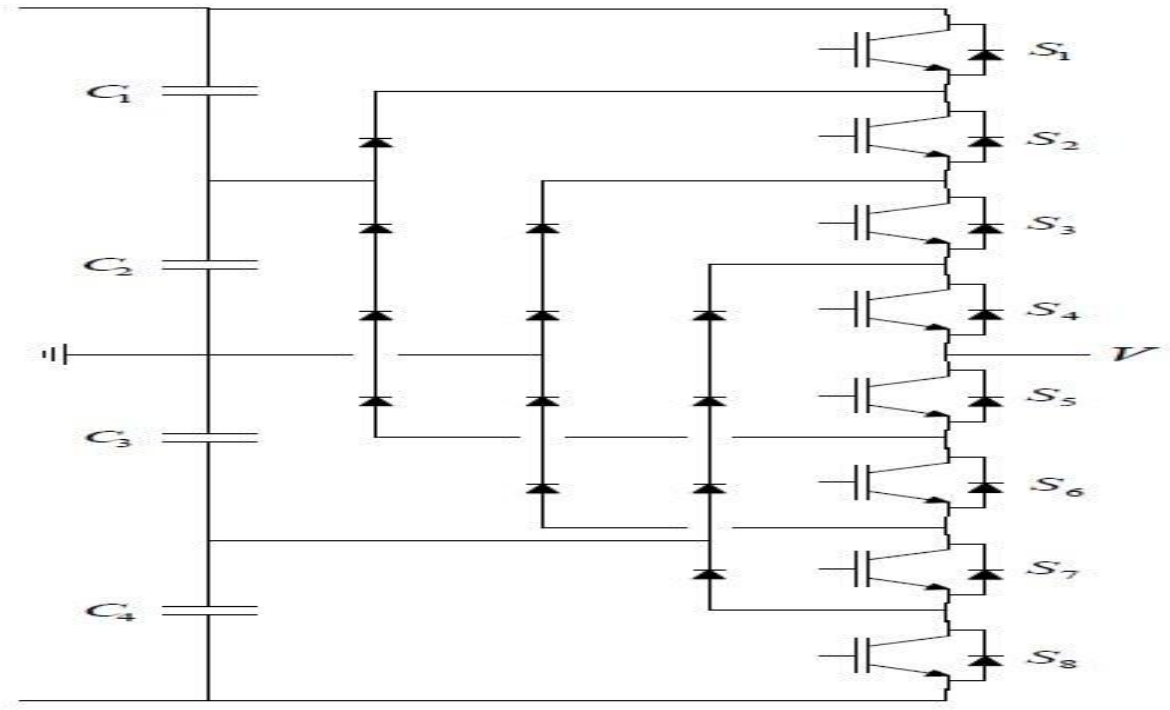

Fig. 4One phase of a diode clamped inverter

III. Simulation Results.

In order to reduce the overall number of switching devices in conventional multilevel inverter topologies, a new topology has been proposed. The novel topology uses less number of switches, keeping efficiency high and THD close to 15%.

A. Power Circuit
A single phase simplified multilevel inverter has the following merits over other existing multilevel inverter topologies.
1. Improved output waveforms.
2. Reduced number of switches employed.
3. Less complexity of the circuit as the levels increase.
4. Smaller filter size.
5.Lower electromagnetic interference and total harmonic distortion.

In addition to this, the capacitors are connected in parallel with the main DC power supply,no significant capacitor voltage swing is produced during normal operation, avoiding a problem that can limit operating range in some other multilevel configurations.

B.Power Circuit Description
The proposed single phase simplified eleven-levelinverter was developed from the five-level inverter. It consists of a single phase conventional H-bridge inverter, four bidirectional switches and a capacitor voltage divider formed by CI. C2, C3, C4, C5. The auxiliary switches formed by the controlled switch S5, S6, S7, S8 and with sixteen diodes D1 to D16.

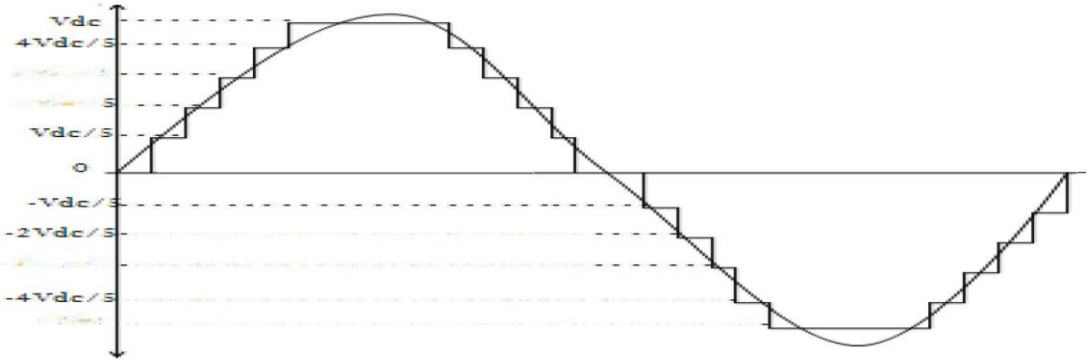

Fig.5 Eleven-level inverter output wave form.

The inverter is capable of producing eleven levels of outputvoltages(Vdc,4Vdc/5,3Vdc/5,2Vdc/5, Vdc/5,0,-Vdc/5, 2Vdc/5,-3Vdc/5,-4Vdc/5,-Vdc) from the DC supply voltage Vdc shown in Fig.5.
There are eleven modes of operation in which two switches conduct for every modes of operation, while other switches remains in OFF position Thedifferent voltage levels of the inverter can be synthesized from the following modes of operation and can be understood using Table. II There are eleven modes of operation in which two switches conduct for every modes of operation, while other switches remains in OFF position The MATLAB/Simulink model of Eleven level Inverter is shown in the Fig. 6.The different voltage levels of theinverter can be synthesized from the following modes of operation and can be understood using Table. II
1. Mode I Operation:
During mode I operation switches S 1 and S4 are turnedON providing an output voltage level of V dc volts.2. Mode II Operation:
During mode II operation switches S4 and S5 are turnedON providing an output voltage level of 4 V dc/5 volts.
3 Mode III Operation:
During mode III operation switches S4 and S6 areturned ON providing an output voltage level of 3Vdc/5 volts .
4. Mode IV Operation:
During mode IV operation switches S4 and S7 areturned ON providing an output voltage level of 2Vdc/5 volts.
5. Mode V Operation:
During mode V operation switches S4 and S8 are turned ON providing an output voltage level of Vdc/5 volts.
6. Mode VI Operation:
This mode of operation has two possible switchingcombinations. Either switches S3 and S4 ar

Vo	S1	S2	S3	S4	S5	S6	S7	S8
Vdc	1	0	0	1	0	0	0	0
4Vdc/5	0	0	0	1	1	0	0	0
3Vdc/5	0	0	0	1	0	1	0	0
2Vdc/5	0	0	0	1	0	0	1	0
Vdc/5	0	0	0	1	0	0	0	1
0	1	1	0	0	0	0	0	0
0*	0	0	1	1	0	0	0	0
-Vdc/5	0	1	0	0	1	0	0	0
-2Vdc/5	0	1	0	0	0	1	0	0
-3Vdc/5	0	1	0	0	0	0	1	0
-4Vdc/5	0	1	0	0	0	0	0	1
-Vdc	0	1	1	0	0	0	0	0

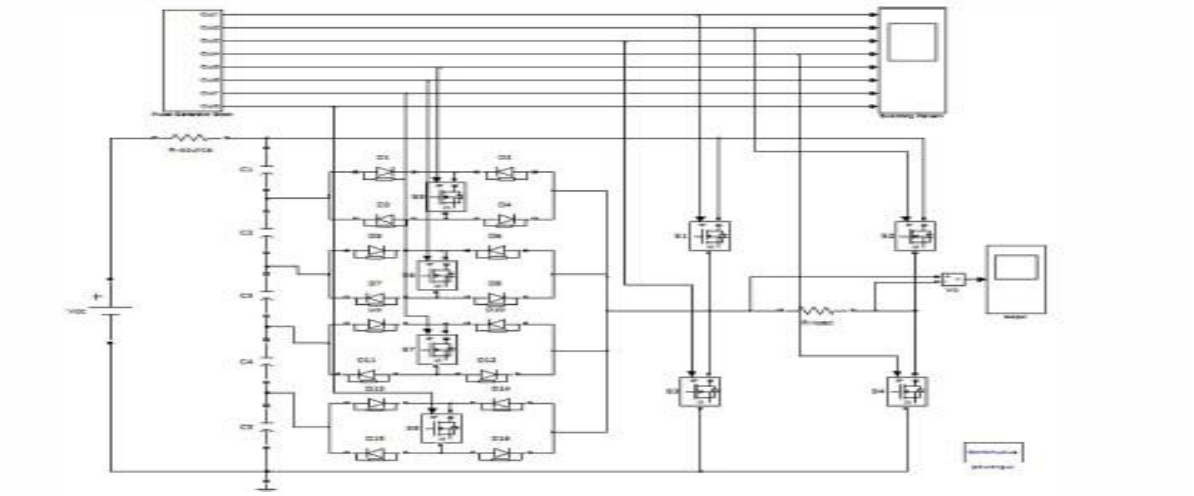

Fig.6Schematic ofEleven Level Inverter

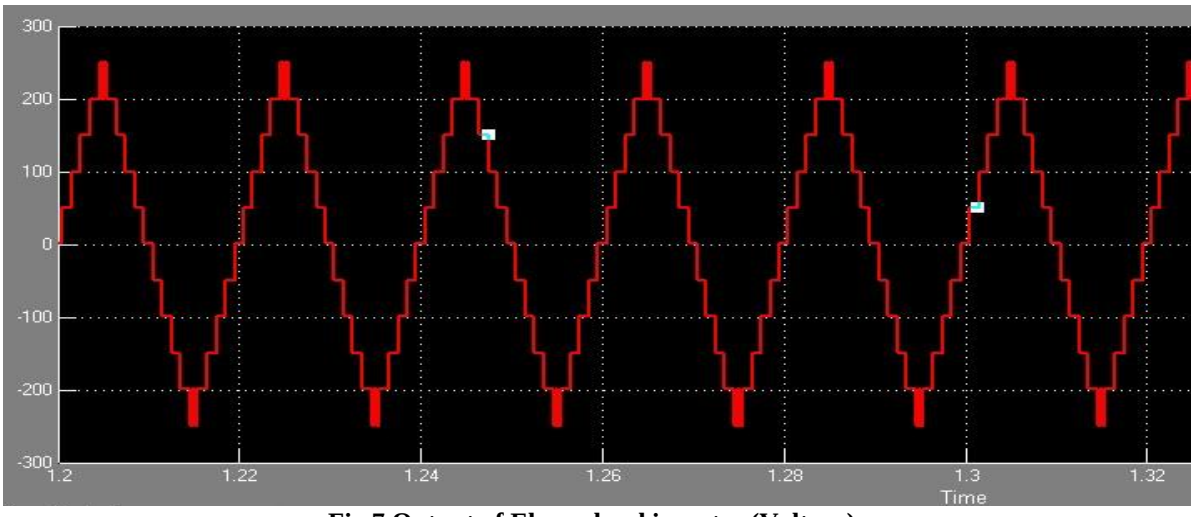

Fig.7 Output of Eleven level inverter (Voltage)

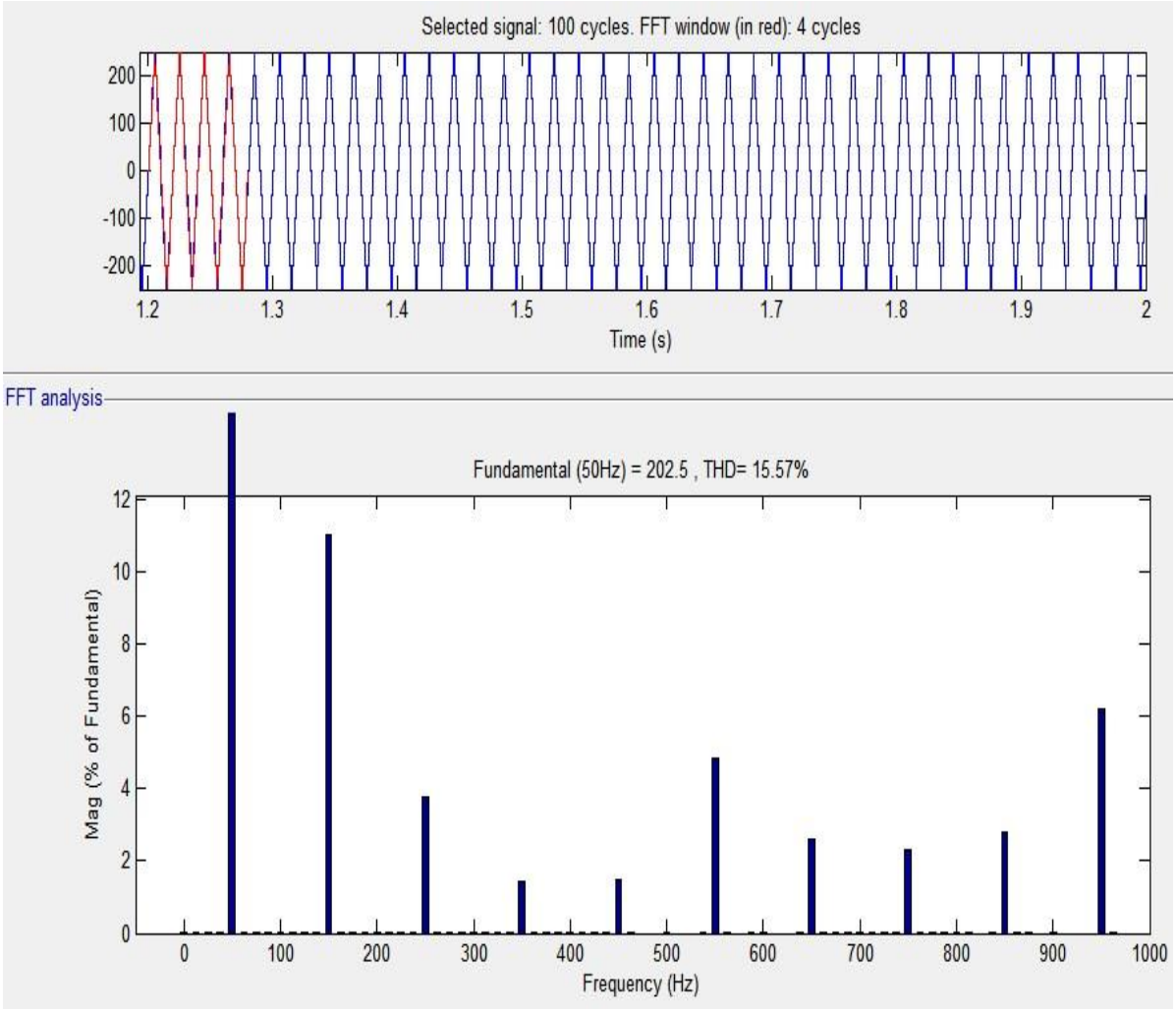

Fig.8FFT analysis

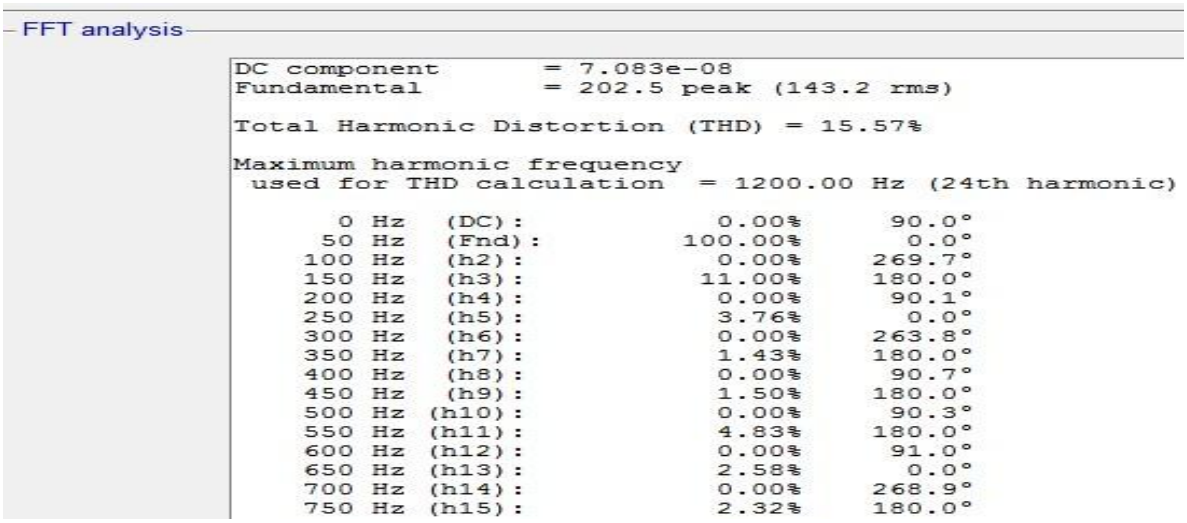

Fig.9 FFT analysis with DC component

IV. Conclusion

A new family of multilevel inverters has been presented and built in MATLAB-Simulink. Multilevel inverters offerimproved output waveforms and lower THD. The output waveform shown in the Fig. 7 is close to sinewave.The novel topology uses less number of switches keeping switching losses minimum.The Total Harmonic Distortion (THD) of the eleven- levelinverter is observed that 15.57% and fundamental voltage is202.5V(50Hz)that has been illustrated in Fig.8.and Fig. 9 with efficiency of 81% .The DC component in the novel topology is low which is illustrated in Fig. 9. The 7^{th} harmonic component which is problematic for Induction motor is low. By using selective harmonic elimination methods the third harmonic component can be eliminated easily to reduce the THD% close to acceptable value of less than 5%. The inverter model developedwas shown to provide accurate results and provided valuableinsight into eleven-level inverter performances.which has superior salient features over conventional topologies in terms of the power switches count and isolated dc supplies, control requirements, cost, and reliability. It is shown that this topology can be a good candidate for converters used in power applications such as renewable systems, FACTS, UPS, etc. Using the novel topology higher level inverters like 17 level can be designed easily to reduce the THD% further. The main advantages of multilevel inverters are the series connection allows higher voltage without increasing voltage stress on switches, Higher voltage capability, Higher power quality, Lower switching losses and its achieved lower harmonic distortion due to more levels of the output waveform.

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